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| 10/699,311 | 10/30/2003 | James C. Fye | H0005246 (256.155US1) | 3928 |

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| EXAMINER | |
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| SMITH, CHENEA | |
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/699,311 | FYE, JAMES C. | |
| | Examiner | Art Unit | |
| | Chenea P. Smith | 2623 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *30 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/15/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 112*

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-29 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites, "an N number of video channels", in lines 1-2, "an N number of video decoders", in line 3, and "a P number of video processing pipelines" in line 6. Claim 1 is vague because "N" and "P" are not defined, and their values are undetermined.

Claim 7 recites, "N number of video channels" in line 1, "N number of video decoders" in line 3, and "P number of video processing pipelines" in line 7. Claim 7 is vague because "N" and "P" are not defined, and their values are undetermined.

Claim 14 recites, "an N number of video channels" in line 3, "an N number of video decoders" in line 7, and "a P number of video processing pipelines" in lines 9-10. Claim 14 is vague because "N" and "P" are not defined, and their values are undetermined.

Claim 19 recites, "N number of video channels" in lines 1-2, "N number of video sources" in line 3, "N number of video decoders" in line 6, and "a P number of video processing

pipelines" in line 9. Claim 19 is vague because "N" and "P" are not defined, and their values are undetermined.

Claim 29 recites, "approximately at least P/2". Claim 29 is vague because P is simply a number that is never specified. Therefore, in order to advance prosecution on the merits, the phrase "the rate of operation is approximately at least P/2", as recited, is interpreted as "the rate of operation is approximately at least the half the number of video processing pipelines ".

Any claims that are not specifically addressed above are being rejected as incorporating the deficiencies of the claim upon which they depend.

***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 7 and 11-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Reitmeier (US6118498, hereinafter Reitmeier).

Regarding claims 1 and 7, Reitmeier discloses an apparatus for display of video data from a designated number of an N number of video channels, the apparatus comprising an N number of video decoders (video decoders 15A, 15B and 45 , see col 3, lines 51-57 and Fig. 1) to receive the video data from the N number of video channels (see col 3, lines 39-41 and Fig. 1), a

designated number of the N number of video decoders to decode the video data from the designated number of the N number of video channels (see col 3, lines 51-57 and Fig. 3), and a P number of video processing pipelines (aux demux processing unit 30 and main transport demux unit 35) coupled to the N number of video decoders through a switch network (switch 20, see Fig. 1), the switch network configured to connect any of the outputs from the N number of video decoders to any of the inputs into the P number of video processing pipelines (see col 3, lines 60-67).

Regarding claim 11, Reitmeier discloses decoding, with an N number of video decoders, a part of video data received in an N number of video channels comprising decoding, with the N number of video decoders, a frame in the video data received in the N number of video channels (see col 3, lines 51-57 and col 5, lines 41-43).

Regarding claim 12, Reitmeier discloses decoding, with an N number of video decoders, a part of video data received in an N number of video channels comprising decoding, with the N number of video decoders, a field of a frame in the video data received in the N number of video channels (a field of the I-frame is inherently decoded because the whole I-frame is decoded, see col 3, lines 51-57 and col 5, lines 41-43).

Regarding claim 13, Reitmeier discloses decoding, with an N number of video decoders, a part of video data received in an N number of video channels comprising decoding, with the N number of video decoders, a scaled field of a frame in the video data received in the N number of video channels (see col 5, lines 62-65 and col 6, lines 5-7).

*Claim Rejections - 35 USC § 103*

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 2-5 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reitmeier (US6118498, hereinafter Reitmeier), as applied to claims 1 and 7 above, and further in view of Machida et al. (EP1158788, hereinafter Machida).

Regarding claim 2, Reitmeier does not specifically disclose an image size/location logic to receive a designated size of a display window and the designated number of the N number of video channels whose video data is to be displayed in the display window, the image size/location logic to determine a location in the display window and a size of a part of the display window for display for the video data for each of the designated number of video channels.

In an analogous art, Machida discloses an image size/location logic (image selection means 101/adapted image synthesization means 105/screen control means 106, see Fig. 3) to receive a designated size of a display window (display window size must be designated since the sizes of the images are designated in proportion to the screen size, see col 5, lines 17-23) and the designated number of the N number of video channels whose video data is to be displayed in the

display window (see col 5, lines 28-35), the image size/location logic to determine a location in the display window (see col 5, lines 56-58 and col 6, line 1) and a size of a part of the display window for display for the video data for each of the designated number of video channels (see col 5, lines 17-23).

It would have been obvious for a person having ordinary skill in the art at the time of the invention to modify Reitmeier's system to include an image size/location logic to receive a designated size of a display window and the designated number of the N number of video channels whose video data is to be displayed in the display window, the image size/location logic to determine a location in the display window and a size of a part of the display window for display for the video data for each of the designated number of video channels, as disclosed by Machida, for the advantage of providing flexibility to a system in order to effectively display multiple screens within a display.

Regarding claim 3, Reitmeier in view of Machida discloses an N number of scalers (image processing means 102, see Machida, Fig. 3), wherein a designated number of the N number of scalers are to scale decoded video data from a designated number of the N number of video channels (see Machida, col 5, lines 36-41 and Fig. 3) based on the determined size of the part of the display window (see Machida, col 5, lines 17-23).

Regarding claim 4, Reitmeier in view of Machida discloses a P number of video processing pipelines (aux demux processing unit 30 and main transport demux unit 35, see Reitmeier, Fig. 1) to process decoded video data of a designated number of the video channels received from a designated number of N number of video decoders (see Reitmeier, col 3, lines 60-67).

Regarding claims 5 and 8, Reitmeier discloses a P number of video processing pipelines and an N number of video decoders (see Fig. 1), but does not specifically disclose P less than N.

In an analogous art, Machida discloses P number of video processing pipelines (image processing means 102), and discloses P less than N (Machida's system selects specific channels among all of the channels received, see col Machida, 4, lines 55-58. The number of video processing pipelines are equal to the number of channels selected, not the number of channels input, and therefore, the P number of video processing pipelines is less than an N number of video decoders, see Machida, col 4, lines 57-58 and col 5, lines 1-4) and a display/control logic (screen control means 106) to control a process order of a designated number of N number of video channels by P number of video processing pipelines (see col 5, lines 17-19).

It would have been obvious for a person having ordinary skill in the art at the time of the invention to modify Reitmeier's system to include a P number of video processing pipelines less than an N number of video decoders, as disclosed by Machida, for the advantage of reducing the overall size of the apparatus.

7. Claims 6 and 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reitmeier (US6118498, hereinafter Reitmeier), as applied to claims 1 and 7 above, and further in view of Miyazaki et al. (US5883676, hereinafter Miyazaki).

Regarding claim 6, Reitmeier disclosed processed decoded video data and a P number of video processing pipelines (see Fig. 1), but does not specifically discloses a write multiplexer receiving data, the write multiplexer storing the data into a memory.

In an analogous art, Miyazaki discloses a write multiplexer (multiplexer 12) receiving data, the write multiplexer storing the data into a memory (VRAM, see Fig. 1).

It would have been obvious for a person having ordinary skill in the art at the time of the invention to modify Reitmeier's system to include a write multiplexer receiving data, the write multiplexer storing the data into a memory, as disclosed by Miyazaki, for the advantage of sequentially storing I-frames as they are decoded, thereby reducing the latency of switching signals.

Regarding claim 9, Reitmeier in view of Miyazaki discloses storing a processed decoded part of the video data in the N number of video channels (see Reitmeier, col 3, lines 51-57 and col 5, lines 41-43) into a part of a video buffer that is not updating the display (see Miyazaki, col 7, lines 44-67 and col 8, lines 1-14).

Regarding claim 10, Reitmeier in view of Miyazaki discloses switching the part of the video buffer that is not updating the display with a part of the video buffer that is updating the display, upon determining that the P number of video processing pipelines (aux demux processing unit 30 and main transport demux unit 35, see Reitmeier, Fig. 1) has completed processing the decoded part of the video data for each of the N number of video channels (see Miyazaki, col 7, lines 44-67 and col 8, lines 1-14).

8. Claim 14 rejected under 35 U.S.C. 103(a) as being unpatentable over Reitmeier (US6118498, hereinafter Reitmeier) in view of Machida et al. (EP1158788, hereinafter Machida) and further in view Klosterman (US6453471, hereinafter Klosterman) and Miyazaki et al. (US5883676, hereinafter Miyazaki).

Regarding claim 14, Reitmeier in view of Machida discloses a method comprising receiving a location in a display (see Machida, col 5, lines 56-58), receiving a designated number of an N number of video channels to be displayed (see Reitmeier, col 3, lines 51-57), and performing the following for each of the designated number of the N number of video channels:

decoding, with one of an N number of video decoders, a frame of video data received in the video channel (see Reitmeier, col 3, lines 51-57 and col 5, lines 41-43),

inputting the decoded frame into one of a P number of video processing pipelines (main transport demultiplexer 35, see Reitmeier, col 4, lines 10-11) through a non-blocking switch network (see Reitmeier, col 3, lines 66-67),

processing, by the one of the P number of video processing pipelines, the decoded frame, and storing the processed decoded frame into a part of a video buffer (see Reitmeier, col 3, lines 66-67 and col 4, lines 63-65).

Reitmeier in view of Machida does not specifically disclose receiving an image size of an image in which a channel is to be displayed, or a part of a video buffer that is not updating the display.

In an analogous art, Klosterman discloses receiving an image size of an image in which a channel is to be displayed (see col 10, lines 54-56).

It would have been obvious for a person having ordinary skill in the art at the time of the invention to modify the system of Reitmeier in view of Machida to include receiving an image size of an image in which a channel is to be displayed, as disclosed by Klosterman, for the advantage of ensuring that the entire picture would be viewable.

Reitmeier in view of Machida, and further in view of Klosterman does not specifically disclose a part of a video buffer that is not updating the display.

In an analogous art, Miyazaki discloses a part of a video buffer that is not updating the display (see col 7, lines 44-67 and col 8, lines 1-14).

It would have been obvious for a person having ordinary skill in the art at the time of the invention to modify the system of Reitmeier in view of Machida, and further in view of Klosterman to include a part of a video buffer that is not updating the display, as disclosed by Miyazaki, for the advantage reducing the latency of switching signals.

9. Claims 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reitmeier (US6118498, hereinafter Reitmeier) in view of Machida et al. (EP1158788, hereinafter Machida), and further in view Klosterman (US6453471, hereinafter Klosterman) and Miyazaki et al. (US5883676, hereinafter Miyazaki), as applied to claim 14 above, and further in view of Miura et al. (US6456335, hereinafter Miura).

Regarding claim 15, Reitmeier in view of Machida, and further in view of Klosterman and Miyazaki discloses processing, by the one of a P number of video processing pipelines, a decoded frame (see Reitmeier, col 3, lines 51-57 and col 5, lines 41-33), but does not specifically disclose determining whether a video channel is in a failed state.

In an analogous art, Miura discloses determining whether a video channel is in a failed state (see col 18, lines 56-63 and col 19, lines 1-9).

It would have been obvious for a person having ordinary skill in the art at the time of the invention to modify the system of Reitmeier in view of Machida, and further in view of Klosterman and Miyazaki to include executing a video fail operation if one of an N number of video decoders does not lock onto video data from one of an N number of video channels after a predetermined time, as disclosed by Miura, for the advantage of eliminating unstable conditions of the system, and thereby improving the efficiency of the system.

Regarding claim 16, Reitmeier in view of Machida, and further in view of Klosterman, Miyazaki and Miura discloses processing, by one of a P number of video processing pipelines (main transport demux unit 35, see Reitmeier, Fig. 1), a decoded frame comprising outputting a blacked out frame for the video channel upon determining that the video channel is in a failed state (see col 20, lines 49-54).

Regarding claim 17, Reitmeier in view of Machida, and further in view of Klosterman, Miyazaki and Miura discloses switching a part of a video buffer that is not updating the display with a part of a video buffer that is updating the display, upon determining that the P number of video processing pipelines (aux demux processing unit 30 and main transport demux unit 35, see Reitmeier, Fig. 1) has completed processing the decoded part of the video data for each of the N number of video channels (see Miyazaki, col 7, lines 44-67 and col 8, lines 1-14).

Regarding claim 18, Reitmeier in view of Machida, and further in view of Klosterman, Miyazaki and Miura discloses scaling a decoded frame (see Reitmeier, col 5, lines 62-65 and col 6, lines 5-7) based on image size and designated number of the N number of video channels (see Machida, col 5, lines 45-48).

10. Claims 19 and 23-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reitmeier (6118498, hereinafter Reitmeier) in view of Miura et al. (US6456335, hereinafter Miura).

Regarding claim 19, Reitmeier discloses a system for displaying video data from a designated number of N number of video channels on a video display terminal, the system comprising:

a video logic comprising:

an N number of video decoders (video decoders 15A, 15B and 45, see col 3, lines 51-57 and Fig. 1), wherein each of the N number of video decoders is to receive video data from one of an N number of video channels and to decode the video data (see col 3, lines 39-41 and Fig. 1), and

a P number of video processing pipelines (aux demux processing unit 30 and main transport demux unit 35) coupled to the N number of video decoders through a switch network (switch 20, see Fig. 1), the switch network configured to connect any of the outputs from the N number of video decoders to any of the inputs into the P number of video processing pipelines, wherein one of the P number of video processing pipelines is to process the decoded video data from one of the N number of video decoders (see col 3, lines 66-67).

Reitmeier does not specifically disclose an N number of video sources, wherein each of the N number of video sources is to generate video data in a video channel of the N number of video channels.

In an analogous art, Miura discloses an N number of video sources (see Fig. 35), wherein each of the N number of video sources is to generate video data in a video channel of an N number of video channels (see Fig. 35).

It would have been obvious for a person having ordinary skill in the art at the time of the invention to modify Reitmeier's system to include an N number of video sources, wherein each of the N number of video sources is to generate video data in a video channel of the N number of video channels, as disclosed by Miura, for the advantage of providing a system capable of processing video signals from different sources from different locations.

Regarding claim 23, Reitmeier discloses a video processing pipeline (main transport demux unit 35, see Fig. 1), but does not specifically disclose executing a video fail operation if one of an N number of video decoders does not lock onto video data from one of an N number of video channels after a predetermined time.

In an analogous art, Miura discloses executing a video fail operation if one of an N number of video decoders does not lock onto video data from one of an N number of video channels after a predetermined time (see col 18, lines 56-63 and col 19, lines 1-9).

It would have been obvious for a person having ordinary skill in the art at the time of the invention to modify Reitmeier's system to include executing a video fail operation if one of an N number of video decoders does not lock onto video data from one of an N number of video channels after a predetermined time, as disclosed by Miura, for the advantage of eliminating unstable conditions of the system, and thereby improving the efficiency of the system.

Regarding claim 24, Reitmeier in view of Miura discloses a video fail operation comprising an output of a blacked out frame overlaid with a descriptive text to indicate video failure for the one of the N number of video channels (see Miura, col 20, lines 49-54).

Regarding claim 25, Reitmeier in view of Miura discloses a video fail operation comprising an output of a previous image for the one of the N number of video channels overlaid with a descriptive text to indicate video failure (see Miura, col 20, lines 49-54 and col 36, lines 20-33).

Regarding claim 26, Reitmeier in view of Miura discloses analog video data (rf signal, see Reitmeier, Fig. 1).

11. Claims 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reitmeier (6118498, hereinafter Reitmeier) in view of Miura et al. (US6456335, hereinafter Miura), as applied to claim 19 above, and further in view of Machida et al. (EP1158788, hereinafter Machida).

Regarding claim 20, Reitmeier in view of Miura does not specifically disclose an image size/location logic to receive a designated size of a display window and the designated number of the N number of video channels whose video data is to be displayed in the display window, the image size/location logic to determine a location in the display window and a size of a part of the display window for display for the video data for each of the designated number of video channels.

In an analogous art, Machida discloses an image size/location logic (image selection means 101/adapted image synthesization means 105/screen control means 106, see Fig. 3) to receive a designated size of a display window (display window size must be designated since the sizes of the images are designated in proportion to the screen size, see col 5, lines 17-23) and the designated number of the N number of video channels whose video data is to be displayed in the display window (see col 5, lines 28-35), the image size/location logic to determine a location in the display window (see col 5, lines 56-58 and col 6, line 1) and a size of a part of the display window for display for the video data for each of the designated number of video channels (see col 5, lines 17-23).

It would have been obvious for a person having ordinary skill in the art at the time of the invention to modify the system of Reitmeier in view of Miura to include an image size/location logic to receive a designated size of a display window and the designated number of the N number of video channels whose video data is to be displayed in the display window, the image size/location logic to determine a location in the display window and a size of a part of the display window for display for the video data for each of the designated number of video channels, as disclosed by Machida, for the advantage of providing flexibility to a system in order to effectively display multiple screens within a display.

Regarding claim 21, Reitmeier in view of Miura, and further in view of Machida discloses an N number of scalers (image processing means 102, see Machida, Fig. 3), wherein a designated number of the N number of scalers are to scale decoded video data from a designated number of the N number of video channels (see Machida, col 5, lines 36-41 and Fig. 3) based on the determined size of the part of the display window (see Machida, col 5, lines 17-23).

Regarding claims 22, Reitmeier in view of Miura discloses a P number of video processing pipelines and an N number of video decoders (see Reitmeier, Fig. 1), but does not specifically disclose P less than N.

In an analogous art, Machida discloses P number of video processing pipelines (image processing means 102), and discloses P less than N (Machida's system selects specific channels among all of the channels received, see col Machida, 4, lines 55-58. The number of video processing pipelines are equal to the number of channels selected, not the number of channels input, and therefore, the P number of video processing pipelines is less than an N number of video decoders, see Machida, col 4, lines 57-58 and col 5, lines 1-4) and a display/control logic (screen control means 106) to control a process order of a designated number of N number of video channels by P number of video processing pipelines (see col 5, lines 17-19).

It would have been obvious for a person having ordinary skill in the art at the time of the invention to modify the system of Reitmeier in view of Miura to include a P number of video processing pipelines less than an N number of video decoders, as disclosed by Machida, for the advantage of reducing the overall size of the apparatus.

12. Claims 27-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reitmeier (6118498, hereinafter Reitmeier) in view of Miura et al. (US6456335, hereinafter Miura), as applied to claim 19 above, and further in view of Miyazaki et al. (US5883676, hereinafter Miyazaki).

Regarding claim 27, Reitmeier in view of Miura discloses processed decoded video data and a P number of video processing pipelines (see Reitmeier, Fig. 1), but does not specifically discloses a write multiplexer receiving data, the write multiplexer storing the data into a memory.

In an analogous art, Miyazaki discloses a write multiplexer (multiplexer 12) receiving data, the write multiplexer storing the data into a memory (VRAM, see Fig. 1).

It would have been obvious for a person having ordinary skill in the art at the time of the invention to modify the system of Reitmeier in view of Miura to include a write multiplexer receiving data, the write multiplexer storing the data into a memory, as disclosed by Miyazaki, for the advantage of sequentially storing I-frames as they are decoded, thereby reducing the latency of switching signals.

Regarding claim 28, Reitmeier in view of Miura, and further in view of Miyazaki discloses a clock multiplier network (see Miyazaki, col 13, line 35), the clock multiplier network controlling a rate of operation of the write multiplexer (see col 13, lines 35-37).

Regarding claim 29, Reitmeier in view of Miura, and further in view of Miyazaki discloses a rate of operation of approximately at least P/2 (see Miyazaki, col 13, lines 31-36) .

## *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chenea P. Smith whose telephone number is (571) 272-9524. The examiner can normally be reached on Monday through Friday, 7:30 am - 5:pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chris Grant can be reached on (571) 272-7294. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Chenea P. Smith
9/14/2007

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